



# FDFME3N311ZT

## Integrated N-Channel PowerTrench® MOSFET and Schottky Diode 30 V, 1.8 A, 299 mΩ

### Features

- Max  $r_{DS(on)}$  = 299 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 1.6$  A
- Max  $r_{DS(on)}$  = 410 mΩ at  $V_{GS} = 2.5$  V,  $I_D = 1.3$  A
- Low profile: 0.55 mm maximum in the new package MicroFET 1.6x1.6 **Thin**
- Free from halogenated compounds and antimony oxides
- HBM ESD protection level > 1600 V (Note 3)
- RoHS Compliant



### General Description

This device is designed specifically as a single package solution for a boost topology in cellular handset and other ultra-portable applications. It features a MOSFET with low input capacitance, total gate charge and on-state resistance. An independently connected schottky diode with low forward voltage and reverse leakage current to maximize boost efficiency.

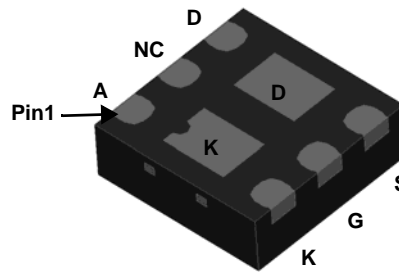
The MicroFET 1.6x1.6 **Thin** package offers exceptional thermal performance for its physical size and is well suited to switching and linear mode applications.

### Application

- Boost Functions

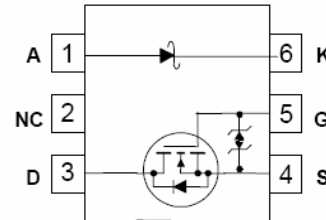


TOP



BOTTOM

MicroFET 1.6x1.6 Thin



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	±12	V
$I_D$	Drain Current -Continuous $T_A = 25$ °C (Note 1a)	1.8	A
	-Pulsed	4.5	
$P_D$	Power Dissipation for Single Operation $T_A = 25$ °C (Note 1a)	1.4	W
	Power Dissipation for Single Operation $T_A = 25$ °C (Note 1b)	0.6	
$V_{RRM}$	Schottky Repetitive Peak Reverse Voltage	28	V
$I_O$	Schottky Average Forward Current	1	A
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range (Note 4)	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Single Operation) (Note 1a)	90	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Single Operation) (Note 1b)	195	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Single Operation) (Note 1c)	110	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Single Operation) (Note 1d)	234	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
1T	FDFME3N311ZT	MicroFET 1.6x1.6 <b>Thin</b>	7"	8mm	5000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		25		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 12\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	0.5	1	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5\text{ V}$ , $I_D = 1.6\text{ A}$		235	299	m $\Omega$
		$V_{GS} = 2.5\text{ V}$ , $I_D = 1.3\text{ A}$		296	410	
		$V_{GS} = 4.5\text{ V}$ , $I_D = 1.6\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		365	603	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 1.6\text{ A}$		2.8		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		55	75	pF
$C_{oss}$	Output Capacitance			15	20	pF
$C_{rss}$	Reverse Transfer Capacitance			7	10	pF
$R_g$	Gate Resistance			7.5		$\Omega$

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 1.6\text{ A}$ , $V_{GS} = 4.5\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		6	12	ns
$t_r$	Rise Time			8	16	ns
$t_{d(off)}$	Turn-Off Delay Time			22	35	ns
$t_f$	Fall Time			1.4	10	ns
$Q_g$	Total Gate Charge			1	1.4	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{GS} = 4.5\text{ V}$ , $V_{DD} = 15\text{ V}$ , $I_D = 1.6\text{ A}$		0.2		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			0.3		nC

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 0.9\text{ A}$ (Note 2)		0.9	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 1.6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		12	22	ns
$Q_{rr}$	Reverse Recovery Charge			3.1	10	nC

**Schottky Diode Characteristics**

$I_R$	Reverse Leakage	$V_R = 28\text{ V}$	$T_J = 25\text{ }^\circ\text{C}$		15	100	$\mu\text{A}$
			$T_J = 85\text{ }^\circ\text{C}$		0.46	4.7	mA
$V_F$	Forward Voltage	$I_F = 1\text{ A}$	$T_J = 25\text{ }^\circ\text{C}$		0.47	0.57	V
			$T_J = 85\text{ }^\circ\text{C}$		0.45		
$V_F$	Forward Voltage	$I_F = 500\text{ mA}$	$T_J = 25\text{ }^\circ\text{C}$		0.38	0.48	V
			$T_J = 85\text{ }^\circ\text{C}$		0.33		

## Electrical Characteristics

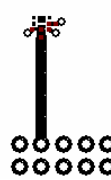
**Notes:**

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.

- (a) MOSFET  $R_{\theta JA} = 90$  °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB.
- (b) MOSFET  $R_{\theta JA} = 195$  °C/W when mounted on a minimum pad of 2 oz copper.
- (c) Schottky  $R_{\theta JA} = 110$  °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5 " x 1.5 " x 0.062" thick PCB.
- (d) Schottky  $R_{\theta JA} = 234$  °C/W when mounted on a minimum pad of 2 oz copper.



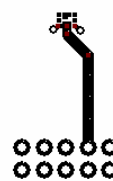
a. 90 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 195 °C/W when mounted on a minimum pad of 2 oz copper.



c. 110 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



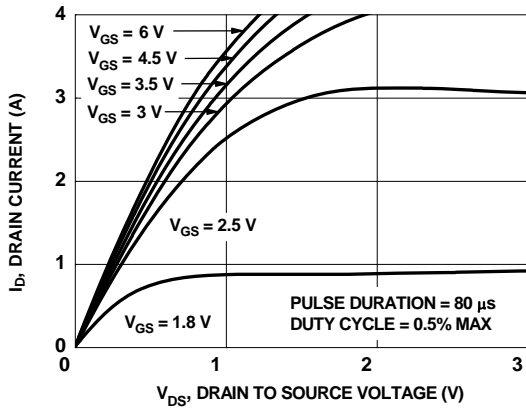
d. 234 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

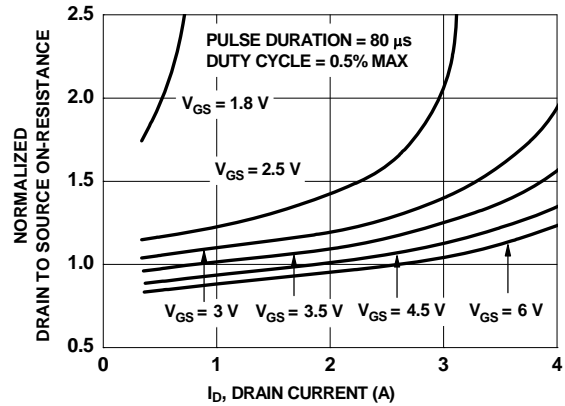
3. The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

4. Rating is applicable to MOSFET only.

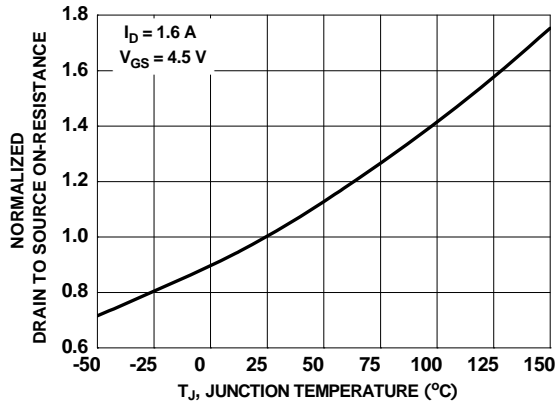
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



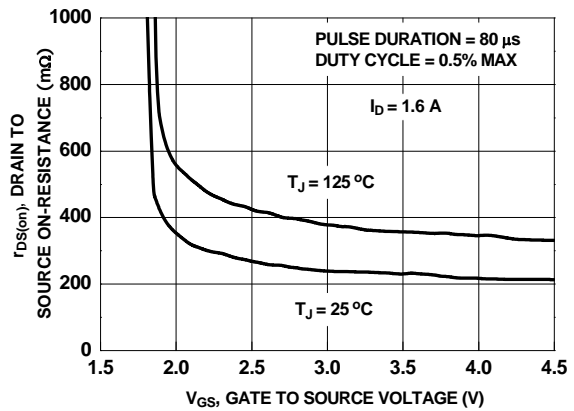
**Figure 1. On Region Characteristics**



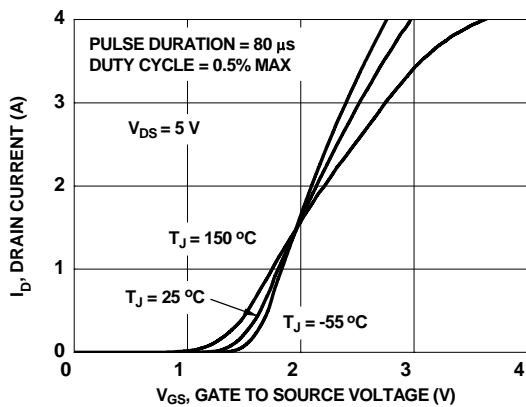
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



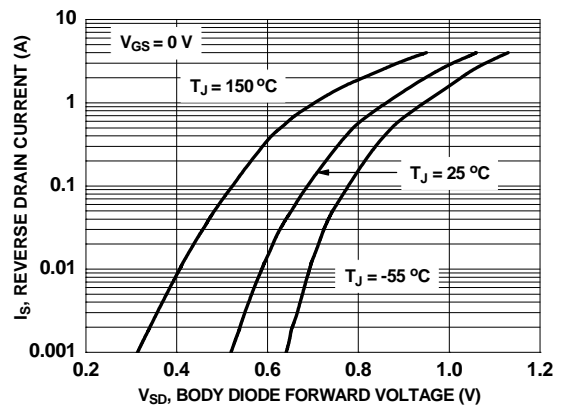
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

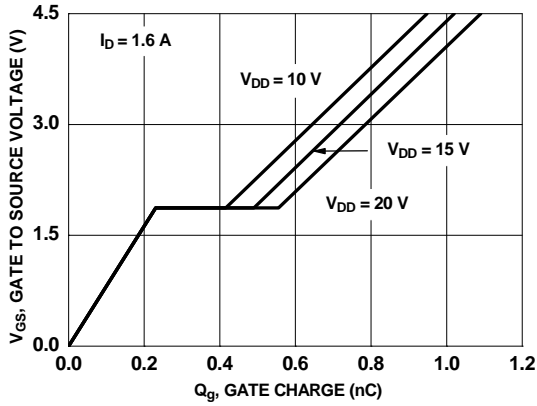


**Figure 5. Transfer Characteristics**

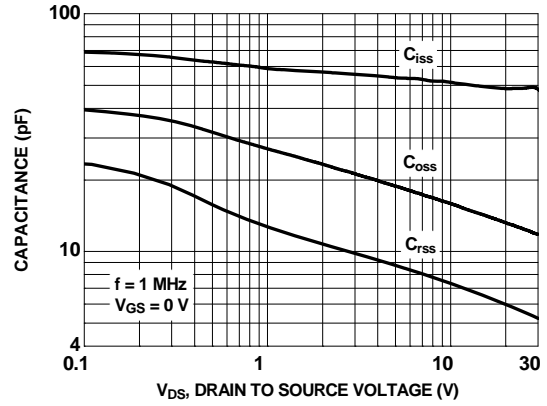


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

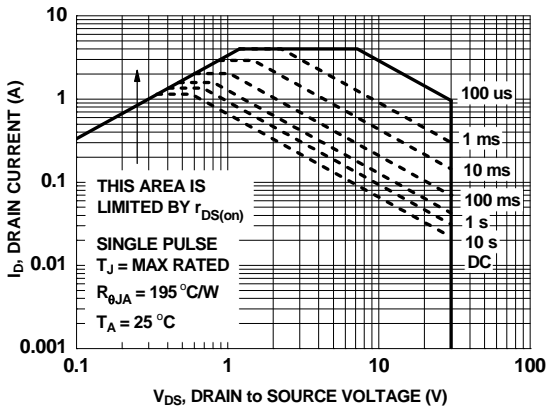
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



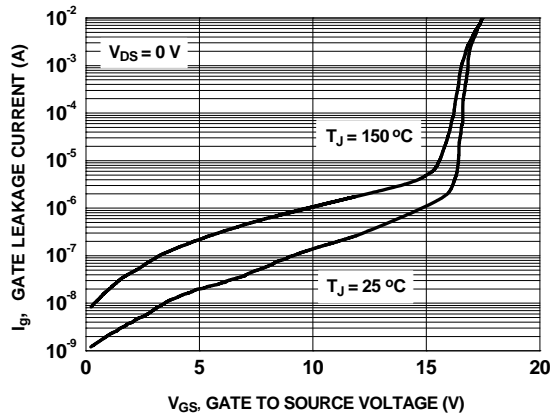
**Figure 7. Gate Charge Characteristics**



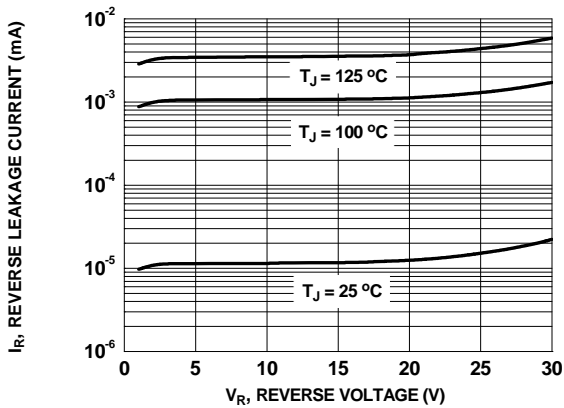
**Figure 8. Capacitance vs Drain to Source Voltage**



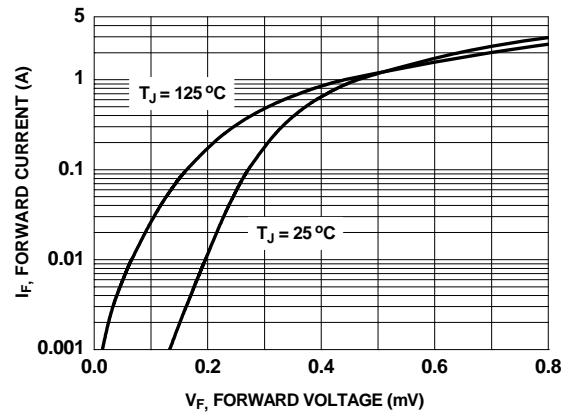
**Figure 9. Forward Bias Safe Operating Area**



**Figure 10. Gate Leakage Current vs Gate to Source Voltage**



**Figure 11. Schottky Diode Reverse Current**



**Figure 12. Schottky Diode Forward Voltage**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

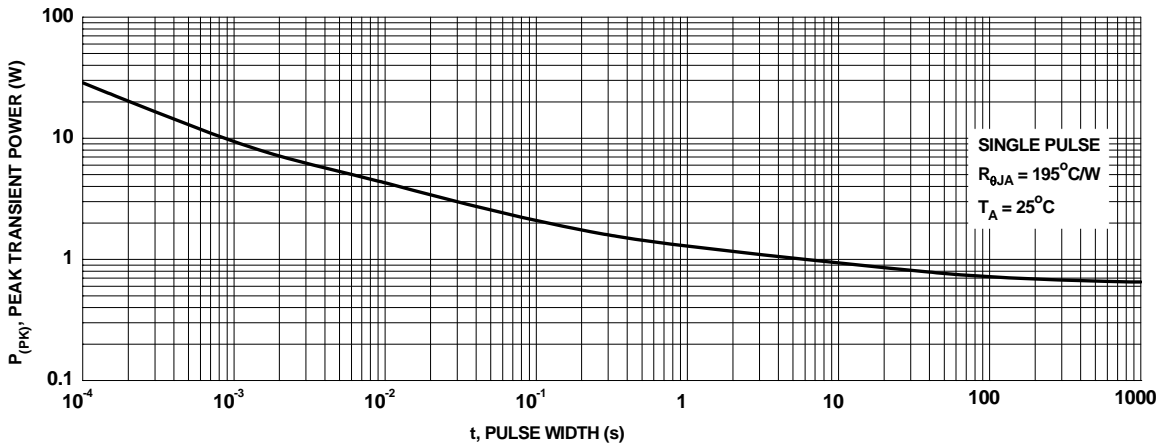


Figure 13. Single Pulse Maximum Power Dissipation

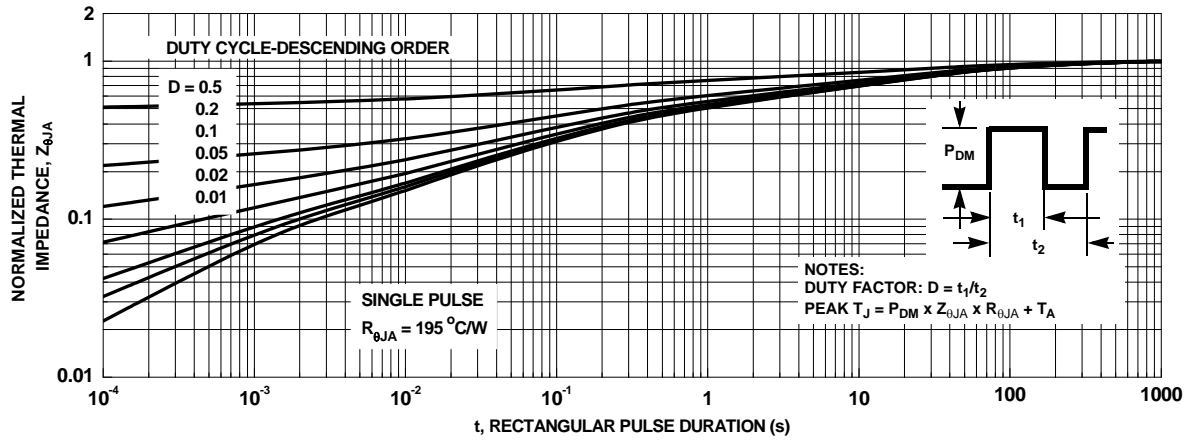
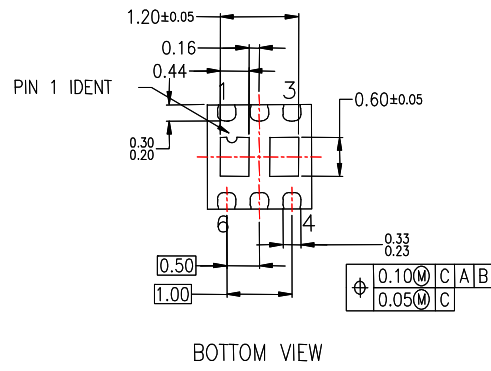
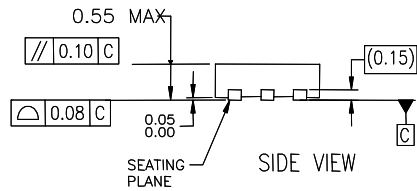
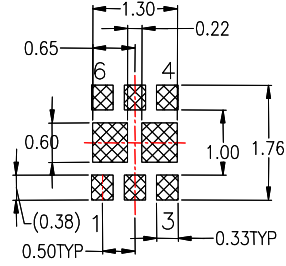
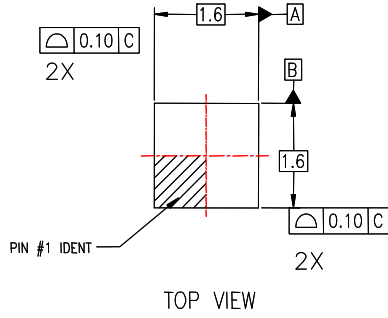


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

### Dimensional Outline and Pad Layout





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